IN THE SPECIFICATION

Please amend the paragraph at page 1, lines 14-28, as follows:

Fig. 10A shows a partial cross-sectional view of a non-punch-through-type and vertical-type IGBT (insulated gate bipolar transistor) taken as a prior art of insulated gate semiconductor device. This IGBT 10 includes an n⁻-type base layer 13, and a p-type base layer 14 formed on the base layer 13. The p-type base layer 14 includes an n+-type source layer (cathode) 15 formed in a selective top surface region thereof. A p+-type drain layer (anode) 11 underlies the bottom surface of the base layer 13 opposite from the top surface thereof. A gate electrode 16 is formed in the base layer 13 so that the gate electrode 16 makes a channel in the p-type base layer 14 for electrical conduction between the source layer 15 and the ~~p-type base layer 14~~ base layer 13. The gate electrode 16 is insulated from the base layer 13, source layer 15 and p-type base layer 14 by an insulating layer 17.

Please amend the paragraph at page 4, lines 13-26, as follows:

An insulated gate semiconductor device according to an embodiment of the invention comprises: a first base layer of a first conduction type; a second base layer of a second conduction type formed on a first surface of the first base layer; a source layer of the first conduction type selectively formed in a surface region of the second base layer; a drain layer of the second conduction type formed on a second surface of the first base layer opposite from the first surface; and a gate electrode insulated from the source layer, the first base layer and the second base layer and forming in the ~~first~~ second base layer a channel electrically connecting the source layer and the ~~second~~ first base layer, wherein ~~the injection efficiency of hole current from said drain layer is 0.27 in maximum~~ the voltage transiently applied to the device is larger than the static breakdown voltage between the source and the drain when a

rated current is turned off under a condition, in which condition the device is connected to an inductance load without using a protective circuit.

Please amend the paragraph at page 4, line 27, to page 5, line 9, as follows:

An insulated gate semiconductor device according to a further embodiment of the invention comprises: a first base layer of a first conduction type; a second base layer of a second conduction type formed on a first surface of the first base layer; a source layer of the first conduction type selectively formed in a surface region of the second base layer; a drain layer of the second conduction type formed on a second surface of the first base layer opposite from said first surface; and a gate electrode insulated from the source layer, the first base layer and the second base layer and forming in the ~~first~~ second base layer a channel electrically connecting between the source layer and the ~~second~~ first base layer, wherein the voltage transiently applied to ~~said device is larger than the static breakdown voltage between the source and the drain when a rated current is turned off under a condition, in which condition an inductance load is from 1 μH to 1mH and said device is connected said inductance load without using a protective circuit, and wherein thickness of the first base layer is 70 μm in maximum~~ the device decreases gradually as a drain current decreases after a rated current is turned off, the voltage transiently applied to the device rising when the rated current is turned off under a condition, in which condition the device is connected to an inductance load without using a protective circuit.

Please amend the paragraph at page 5, lines 10-24, as follows:

An insulated gate semiconductor device according to a still further embodiment of the invention comprises: a first base layer of a first conduction type; a second base layer of a

second conduction type formed on a first surface of the first base layer; a source layer of the first conduction type selectively formed in a surface region of the second base layer; a drain layer of the second conduction type formed on a second surface of the first base layer opposite from said first surface; and a gate electrode insulated from the source layer, the first base layer and the second base layer and forming in the ~~first~~ second base layer a channel electrically connecting the source layer and the ~~second~~ first base layer, wherein ~~the injection efficiency of hole current from the drain layer is less than 9/19~~ a voltage transiently applied to the device is larger than a static breakdown voltage between the source and the drain and decreases gradually as a drain current decreases after a rated current is turned off, the transiently applied voltage rising when the rated current is turned off under a condition, in which condition the device is connected to an inductance load without using a protective circuit.

Please amend the paragraph at page 7, lines 21-37, as follows:

Fig. 1 is a cross-sectional view of a punch-through IGBT 30 taken as an insulated gate semiconductor device according to the first embodiment of the invention. IGBT 30 includes an n^--type base layer 21, and a p-type base layer 14 formed on the n-type base layer 21. The p-type base layer 14 includes an n+-type source layer 15 formed in a selective top surface region thereof. A p-type drain layer (anode) 31 underlies the bottom surface of the n-type base layer 21 opposite from the top surface thereof. A gate electrode 16 is formed in the n-type base layer 21 and in the p-type base layer 14 so as to make a channel in the p-type base layer 14 for electrical conduction between the source layer 15 and the ~~p-type base layer 14~~ n-type base layer 21. The gate electrode 16 is insulated from the n-type base layer 21, source layer 15 and p-type base layer 14 by an insulating layer 17. The p-type base layer 14 and the

source layer 15 are connected to a source electrode 41 (cathode). The drain layer 31 is connected to a drain electrode 42.

Please amend the abstract at page 23, lines 1-14, as follows: